Function and Sensitivity of Signal Processing Systems Based on Addition Followed by Limiting

Erik Johnson and Edward H. Sargent

Abstract—We show for the first time that signal processing schemes based on noncoherent signal addition will require signal transfer characteristics exhibiting high degrees of curvature. We quantify this by proposing a set of single-input, dual-output, power-conserving transfer functions and generating designs based on these characteristics. We then analyze the sensitivity of such a design scheme to nonidealities in the signal level and device behavior, and show that a sampling operation is only possible for transfer characteristics with residual "low" output of less than about 10% and low intensity reflectivity higher than 98%. For single device signal loss of up to 0.1 dB, we show that the best possible crosstalk-to-noise ratio in a packet forwarder (27 dB), is limited by the availibility of the sampling operation.

Index Terms—Nonlinear circuits, optical data processing, optical limiters, optical switches, packet switching.

I. INTRODUCTION

PHOTONIC networks provide abundant information-carrying capacity between points. Increasingly, the optical layer is being used to establish channel-oriented connections, or lightpaths [1], which may be reconfigurable on the timescale of milliseconds. Provisioning, restoration, and traffic-sensitive logical topology reoptimization may be achieved in this manner. Light is playing an increasing role in the higher layers of the networking protocol stack. At present, such lightpaths are too coarse and scalable optical switches too slow to provide packet-by-packet forwarding in the optical domain. This situation is currently addressed using hybrid schemes such as generalized multiprotocol label switching (GMPLS) [2] wherein combined optical and electronic labeling schemes provide the needed granularity and dynamism in the establishment of label-switched paths. It is tempting to ask whether, instead of relying on lookup tables and electronic buffers, in-band labeling could be incorporated into bit streams to enable real-time, on-the-fly forwarding on a packet-by-packet basis. In this scheme, increasingly fast real-time processing of signal will be required, either all-optically, optoelectronically, or electronically.

We investigate here the functional potential, and the sensitivity to real device nonidealities, of a generalized scheme which could afford on-the-fly header processing without buffering and lookup tables. We argue that in such a scheme, a conventional AND function appearing as in Fig. 1(a) and (b) will not be avail-

able, but that a simple one-input-port one-output-port nonlinear transfer function may be achieved, and may be deployed to the same end. This unconventional AND function is a result of photon–photon interactions occurring by nature through a material. This requirement implies that the two signals must occupy the same physical space. If two nonorthogonal signals are in the same spot, an abundance of one signal can masquerade as the presence of the other, and new restrictions must be made on tolerable signal levels. This unconventional AND function—as well as other addition-based logic operations—has been demonstrated in nonlinear optical and optoelectronic devices such as nonlinear directional couplers [3], ultrafast nonlinear interferometers, [4], integrated terahertz optical assymetric demultiplexers [5], wavelength converters [6], and optical hard limiters [7]. Outside of the optical domain, similar behavior exists in ultra-high-speed microwave-frequency electronics using current-driven transistors [8].

Given this promising range of options for implementation, we expore here the generalized function, features, and sensitivity of a scheme in which signal interaction occurs through summation alone, and device output is determined by the input at a single port which is subjected to a limiting transfer function. In this case, the plot of Fig. 1(b) would appear as in Fig. 1(c). An additional output consisting of the remaining signal intensity would appear as shown in Fig. 1(d). To examine the requirements and consequences of performing operations in this fashion, we initially propose a basis set of nonlinear transfer functions which provides the complete desired functionality, and then use a physical device model to generate the degradation of this transfer function. This allows an examination of the design sensitivity to fluctuations in both signal intensity and device nonideality. This analysis sets concrete specifications for the device behavior to enable signal processing operations such as sampling and packet forwarding.

Although the work addresses the general issues of addition-based signal processing, a physical device model must be used to quantify the results. We use a nonlinear optical device—the optical hard limiter [7]—as a model to generate realistic device behavior. Additional challenges arise due the fact that the addition of optical signals is a noncoherent summation process. The 3-dB loss inherent such a summation process is addressed in the work. Although we have used optics to generate the physical models, the results may also be applied to electronic devices whose output current is determined by the total input current, an easily summable quantity. Generally, any device that operates on a single input of a summable quantity will benefit from the analysis.
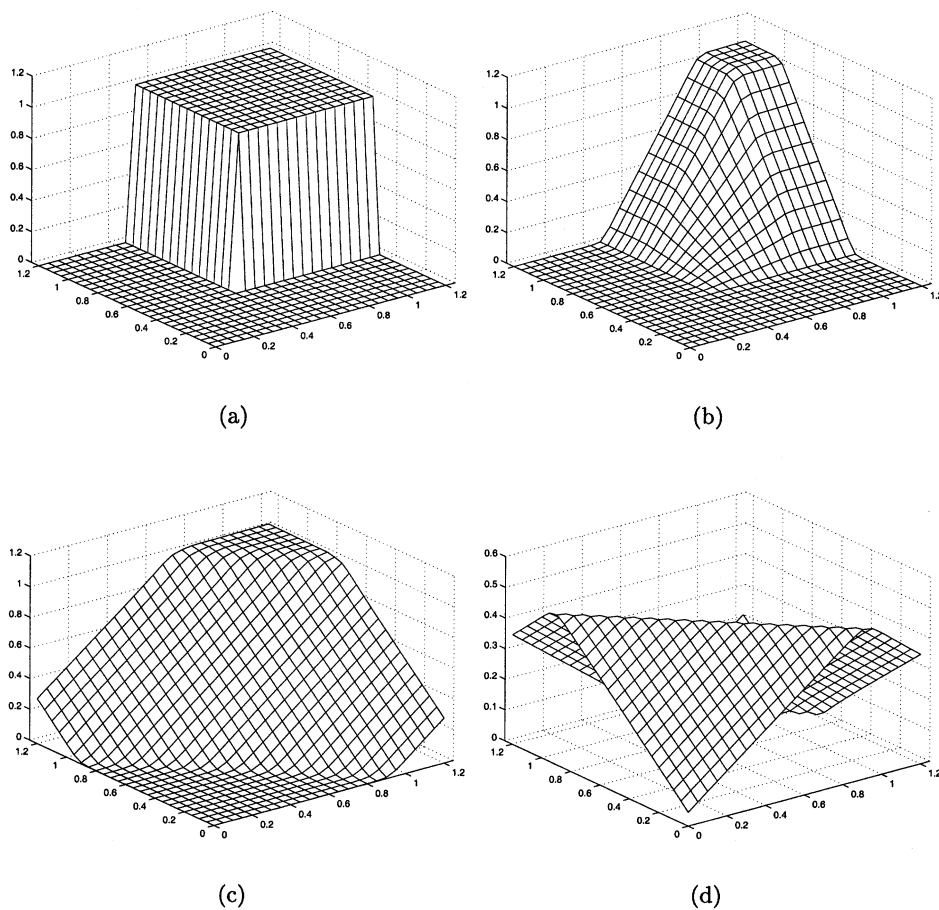
Fig. 1. (a) Output as a function of the two inputs to a typical AND gate. (b) Output when switching behavior is nonideal. (c) Output as a function of the two inputs to an AND gate operating on the summed intensity of the two signals. (d) Total remaining signal intensity, an XOR operation.
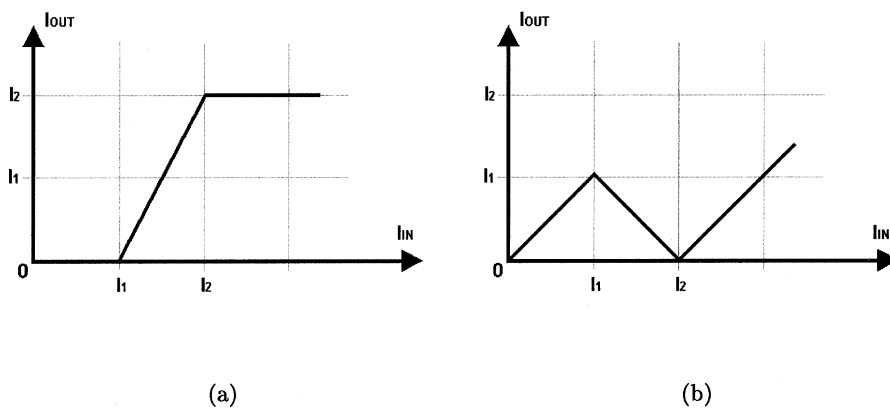

Fig. 2. Basis set of transfer functions. (a) The idealized S-curve. (b) The idealized N-curve.

In this work, we elucidate explicit device-level requirements to make a noncoherent addition-based signal processing scheme feasible and explore how much signal level fluctuation, transfer characteristic smoothness, and device loss can be tolerated or suppressed. We show that a sampler based on this design scheme will be sensitive to large input intensities when a low value has been sampled, and we determine the transfer characteristic sharpness that is necessary. We show that the packet forwarder design is limited in its performance by the restrictions on the sampling operation.

II. DEVICE BEHAVIOR

Relying on the noncoherent addition of signals allows the reduction of Fig. 1(c) and (d) to single-input variable plots in which the input axes are the total input intensity. The nonlinear device behavior that is proposed as the basis set for noncoherent addition signal processing is shown in Fig. 2(a) and (b). These two complementary transfer functions map closely to the behavior of stable optical hard limiters [7], and to a lesser degree, multiple guide nonlinear directional couplers [9].
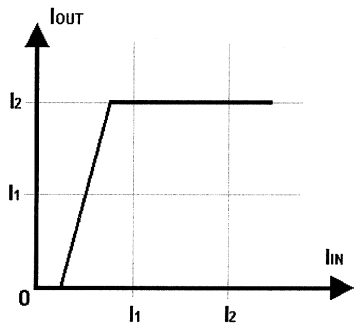
Fig. 3.   Transfer function of module providing small signal gain and signal grooming.

The second inflection point on the S-curve of Fig. 2(a), indicated by I_2, is chosen as the logical high. It can be shown that interconnection of devices exhibiting this behavior alone can provide a complete logic set. When idealized transfer functions are assumed, they can maintain a consistent intensity level for a logical "high." Maintaining this level for a logical "high" requires signal gain to compensate for losses associated with excess loss-free signal splitting, and noncoherent optical addition. Additionally, the gain should be nonlinear, so that small fluctuations around the ideal logic levels are suppressed. This nonlinear gain, with a transfer function as shown in Fig. 3, may be provided in two ways: through gain followed by a device with the S-curve characteristic, or through interconnection of three S-curve devices.

This signal grooming operation is the keystone of the designs. Without this behavior, no suppression of small fluctuations occurs, multiple operations distort the signal levels, and eventually, the data is lost. Each method of providing this operation, however, presents a challenge. The use of a separate source for signal gain entails the integration of another technology onto a chip, and the use of multiple S-curves will result in a large amount of lost bias energy.

Fig. 4(a)–(d) shows the interconnection of the transfer functions and the 3-dB gain module to provide logical operations.

III. SAMPLER AND PACKET FORWARDER DESIGN

We further explored noncoherent addition signal processing through the design and study of a sample-and-hold device and a packet forwarder. Optical sampling has been demonstrated experimentally in bistable devices, essentially performing noncoherent addition of signals, but in keeping with the theme of integration, the work describes achieving this operation using, once again, only the basis set of transfer functions.

To sample an optical signal and hold its value in optical form is an extremely useful operation in all-optical communications networks. Digital sampling enables the use of a high-speed optical signal to perform ultra-fast operations over a time scale greater than a bit length.

The design for a noncoherent addition-based sampler presented in this work is based on an electronic flip-flop design. The topological layout of the sampler is shown in Fig. 5. The design behaves as follows: when the clock signal, CLK, is high, the output varies in proportion with the value presented at the input. When the CLK signal goes low, the feedback from the

output is the selected output value. This value then persists at the output until the CLK signal is made high again. This provides an optical sampling function where the input value is sampled at the moment that the CLK signal falls.

The key elements of the sampler are the inversion operation and the presence of a short delay in the feedback loop. The inversion operation produces a high signal at the input of one of the AND gates when the CLK signal is low. This selects the feedback signal and suppresses the input signal when the CLK is low. The feedback delay allows the output to be selected before the low CLK signal propagates through the system.

The goal of this design is to produce a system that can forward a packet to an output port specified by its address bits. This design considers implementation with and without reconfigurability. The initial design considers a direct hardware mapping of address values to output ports. A more complicated logic scheme in the address decoding section of the design would allow dynamic address-to-port assignment. The use of lookup tables to map ports to absolute addresses is beyond the scope of the present design.

The packet forwarder makes use of the idealized device as a signal segregator. The two outputs of this single-input device are determined by the two derived transfer functions, which allows the physical separation of signals of two different intensities I_1 and I_2. The packet router uses the segregator to separate the packet from its framing bit. This will allow a very simple address recognition scheme and circumvents the need for synchronization.

A packet forwarder must perform the following operations:
- extraction of framing bit,
- extraction of addressing information,
- address decoding,
- routing of packet onto decoded path,
- reassembly of packet and framing signal.

The packets to be processed by the forwarder are formed as shown in Fig. 6. In this packet design, the frame bit is assigned a different intensity level, I_2, than the address and data bits. This enables the separation of the copropagating frame bit using a segregator. This separation operation, and subsequent operations, are described with reference to Fig. 7, a schematic of the packet forward layout.

Once the frame signal has been separated, the address information is extracted by temporally aligning parts of the signal with the framing bit by subjecting copies of the signal to preset time delays. The lengths of these time delays is determined by the data rate of the system. They are set so that the address bits are at the flip-flop inputs when the clocks go low.

The stored address information is decoded according to the preset routing scheme which may be implemented using combinational optical logic to keep consistency with the all-optical strategy. The packet, without the framing bit, then propagates down the correct path as determined by the output address bit. The framing bit, with intensity level 2, then rejoins the packet.

With the packet design shown in Fig. 6, the system is self-clocking and needs no external synchronization. The framing bit gives the reference time against which the arrival times of the rest of the bits are measured. The relative positions of the synchronization, address, and data portions of the packet are

(a)   (b)

(c)   (d)
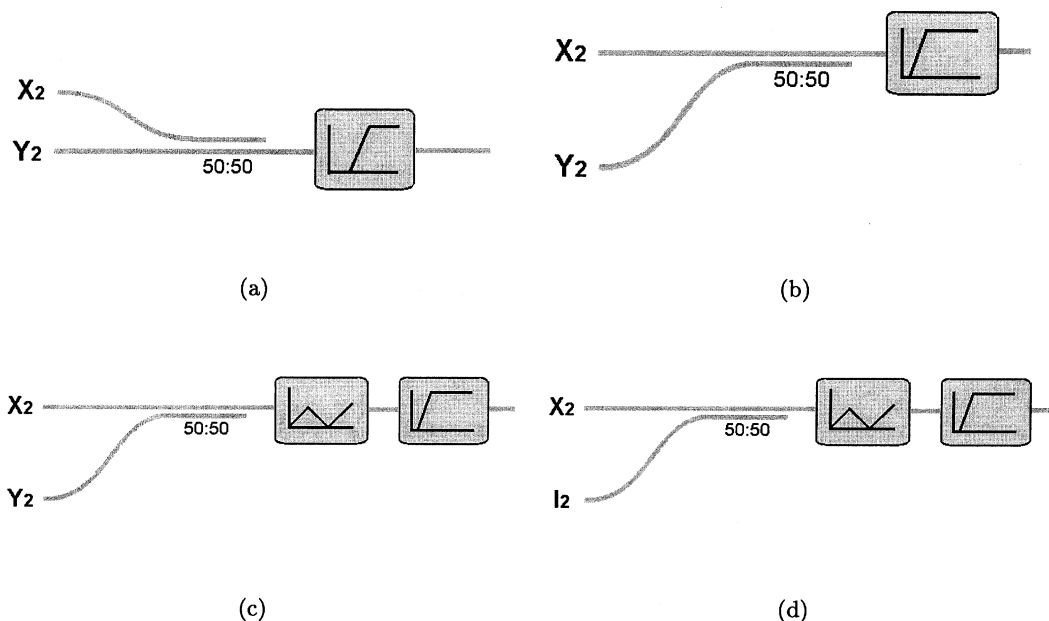
Fig. 4.   Connection of devices to achieve (a) AND, (b) OR, (c) XOR, and (d) NOT layout. The OR, XOR, and NOT operations make use of the 3-dB conversion module.
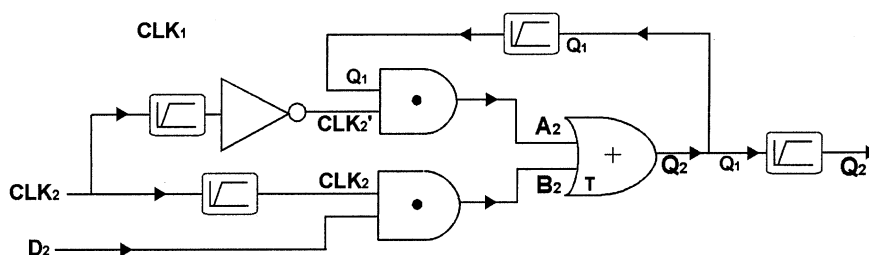

Fig. 5.   Layout of logic gates to enable sampling operation using noncoherent addition of signals. This design relies most heavily on the availability of the inversion operation and the signal restoration module.
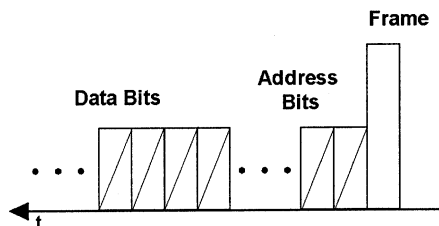

Fig. 6.   Composition of a packet to be routed all-optically. The separation of the data and address bits is enabled by the leading framing bit.

completely arbitrary, and are only determined by the setup of the system.

IV. SENSITIVITY ANALYSIS OF DESIGNS

The designs proposed in the preceding section assumed an idealized transfer function. A goal of this work is to establish a link between device-level performance and system-level performance for this signal-processing scheme. To perform this analysis, the device behavior was modeled by that of an optical hard-limiter. The effects of loss and transfer-function smoothness were included in the model. These two sources of nonideality are not independent, however, as the smoothness of the transfer function varies inversely with the length but the loss

scales proportionally. The resulting characteristics for devices of varying lengths are shown in Fig. 8.

Table I generalizes the results of the simulations and lists the important characteristics of each transfer characteristic. For each number of layers, the following parameters are listed: the initial slope (ideally 0), the output intensity when the input intensity is I_1 (ideally 0), the intensity at which the slope first equals 1 (ideally 1), and the limiting intensity (ideally 2).

As well as smoothing in the transfer functions, the effect of linear absorption was also included in the model. A linear loss of 1.74 dB/cm was used, corresponding to the loss observed in poly 1,4-phenylene-1,2-di-phen-oxyphenyl vinylene (DPOP-PPV) (see Fig. 9). This material was chosen as it satisfies both of the materials figures of merit for third-order nonlinear signal processing [10].

The logic gate designs were analyzed to observe how they behave for different numbers of layers with a constant amount of loss. The results of this analysis are presented in Fig. 10. The deisred logical operations are observed, but more importantly, small fluctuations in the signal level on the order of -6 dB are tolerated. This tolerance is better seen when the designs are analyzed in terms of their sensitivity to fluctuations in signal intensity. Results of this study, presented in Fig. 9, show device output-to-input ratios as the signals vary around their ideal
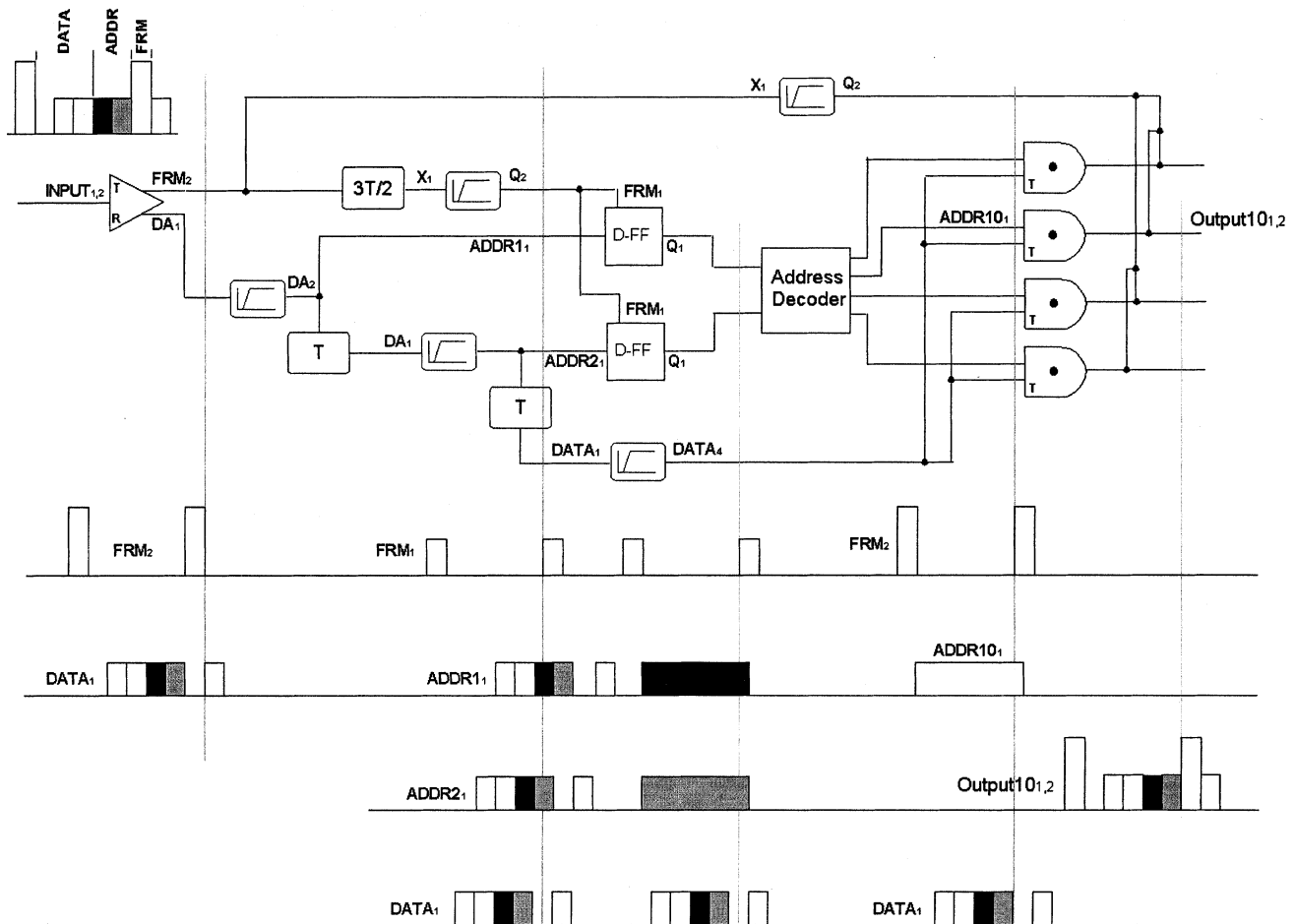
Fig. 7. Schematic of a packet forwarder based on noncoherent signal-addition logic. The packet forwarder separates the framing bit from the packet and uses this signal to trigger the flip-flops, recording the value of the header bits. These bits are decoded to select the correct output port and the packet is forwarded.

TABLE I
MAPPING OF NUMBER OF LAYERS IN SIMULATION TO TRANSFER CHARACTERISTIC PARAMETERS

Number of Layers	Initial Slope	$I_{Out}(I_{In} = I_1)$	I_{In} when slope $= 1$	Limiting Intensity
100	0.66	0.89	0.73	3.1
200	0.24	0.61	0.86	2.54
300	0.07	0.35	0.96	2.31
400	0.02	0.19	0.99	2.21
500	0.005	0.10	1.0	2.12
600	0.002	0.05	1.0	2.08
700	0.001	0.02	1.0	2.08

value. It can be seen that the OR and XOR operations tend to suppress small intensity fluctuations. Values just below the ideal have an output-to-input ratio greater than one, and the signal is amplified. As well, the NOT operation operates correctly for a range of values around the ideal. This is by virtue of the use of the 3-dB gain/normalization module, and because the AND operation does not have this benefit, it always degrades the signal. In short, the OR, XOR, and NOT operations are insensitive to fluctuations on the order of -6 dB due to the action of the normalization stage.

The results which best elucidate the link between device level performance and system behavior are the analyses of the sampler and the packet router. The sampler was analyzed by breaking the feedback loop and observing the nonlinear open loop gain. The results of this study are shown in Fig. 11. For bistability to occur, the curve of Fig. 11 must have portions both above and below the diagonal line representing unity gain. It can be seen that as the device length increases, the additional loss reduces the portion above the line, and eventually this portion completely dissappears. Thus, for a given amount of
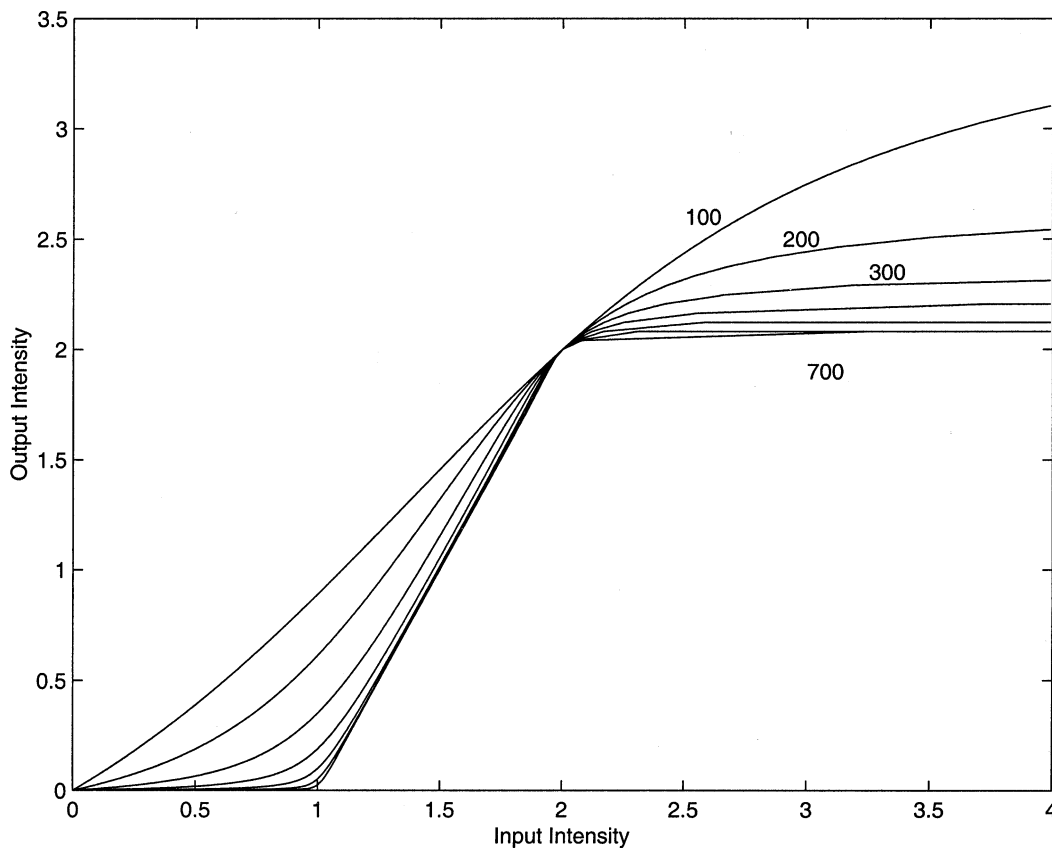
Fig. 8. Simulation results for stable optical hard-limiters as the number of layers changes from 100 to 700. A finite number of layers causes a smoothing effect on the transfer characteristic.
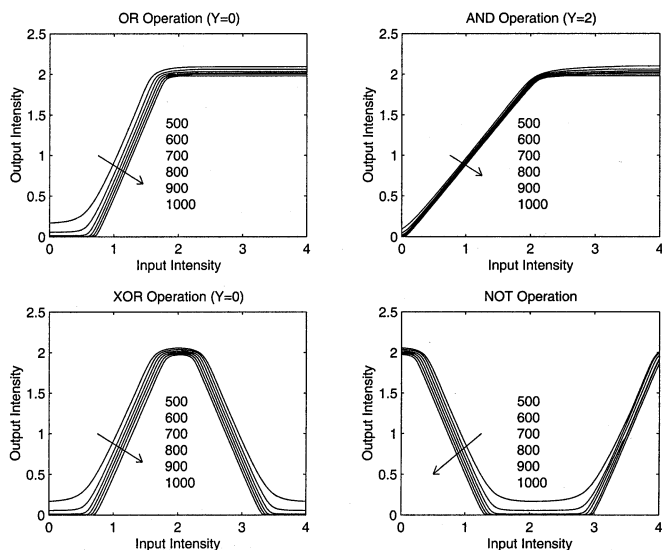

Fig. 9. Output of logic gate configurations as device length varies and losses are appropriate for DPOP-PPV.
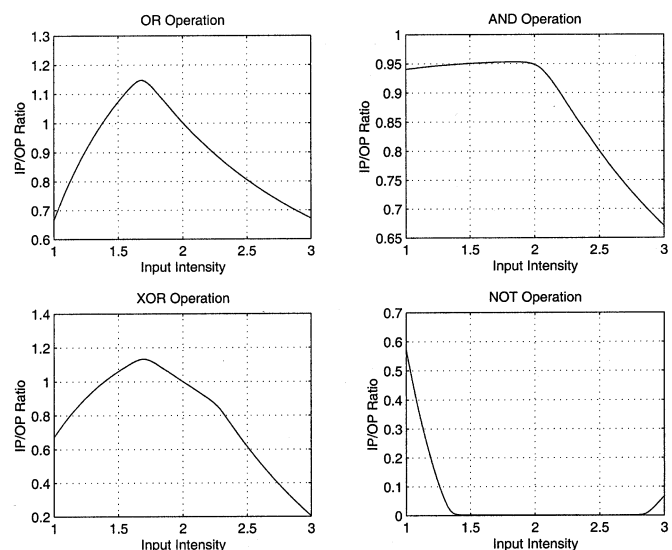

Fig. 10. Input-to-output ratio as a function of input intensity for the four logic gate configurations (800-layer limiter model with loss appropriate for DPOP-PPV).

loss, only a certain device length can be tolerated, and hence there is a maximum to the sharpness that can be exploited.

Another consequence of the signal-processing scheme is the lack of complete suppression of input signals to the sampler. In an ideal sampler, the stored value is completely independent of the input signal once the clock signal has gone low. In the non-coherent signal combination scheme, the nonideality of devices leads to signals bleeding through and appearing at the output. This effect is examined by observing the open-loop behavior
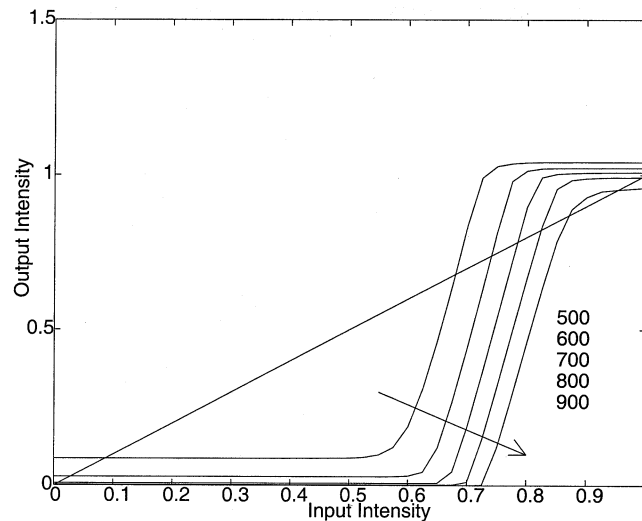
Fig. 11.   Open-loop behavior of sampler for losses appropriate for DPOP-PPV.

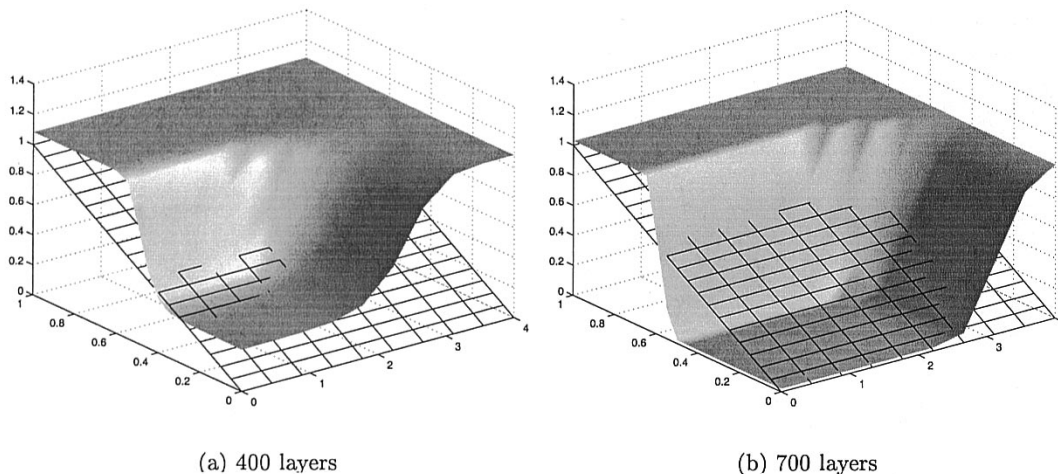(a) 400 layers   (b) 700 layers

Fig. 12.   Open-loop behavior of sampler as input intensity changes. For sampling to occur, the curved surface must have portions both above and below the flat plane representing unity gain. Results shown for (a) 400-layer limiter model and (b) 700-layer limiter model. For both numbers of layers, the sampler fails when sufficiently high power appears at the input. For 400 layers, this failure occurs at an input intensity of 1.8, which is less than the value of a high signal. For the 700-layer limiter model, signals less than 3.1 do not cause the loss of a sampled low value.

of the sampler as the input intensity changes. The results of this study appear in Fig. 12. The figure shows the open-loop gain plotted as the input intensity changes from 0 to I_2. As this change occurs, the point at which the curves cross the unity gain line change. A flat plane representing the unity gain is also shown in Fig. 12. The intersection of these two curves represents the threshold between a high and a low stored signal. When the two planes no longer intersect, there is no regions both above and below the unity gain plane, and sampling no longer occurs. Fig. 12(a) shows the results for a device model corresponding to a 400-layer limiter, and Fig. 12(b) for a 700-layer model.

The failure points for each of these models can be clearly interpreted from the plots. For 400 layers, the failure point occurs at an input intensity of 1.8, which is less than the value of a logical high, 2. This means that a sampler based on devices with behavior similar to the 400-layer limiter model will not operate correctly, as normal signals appearing at the input will cause logical lows to be lost. For the 700-layer limiter model, the failure

point is 3.1, which is greater than a logical high. As long as the incident signals are constrained to be below this level, a sampled logical low will be preserved.

The results of Figs. 11 and 12 have consequences for the packet forwarder design, which we also studied through simulation. One representative result of input and output bit streams is shown in Fig. 13. The single header bit selects port 1 as the desired output port, and the majority of the signal appears at that port. However, a small amount of signal appears at the other port as crosstalk. A graph of signal-to-crosstalk ratio for increasing device lengths is shown in Fig. 14. This graph shows that the signal-to-crosstalk ratio improves as the device length increases, as the transfer function is sharpened. However, the correct performance of the sampler limits the maximum length of the device due to loss. In this way, the individual device loss and the best possible signal-to-crosstalk ratio are linked through the sampler behavior.
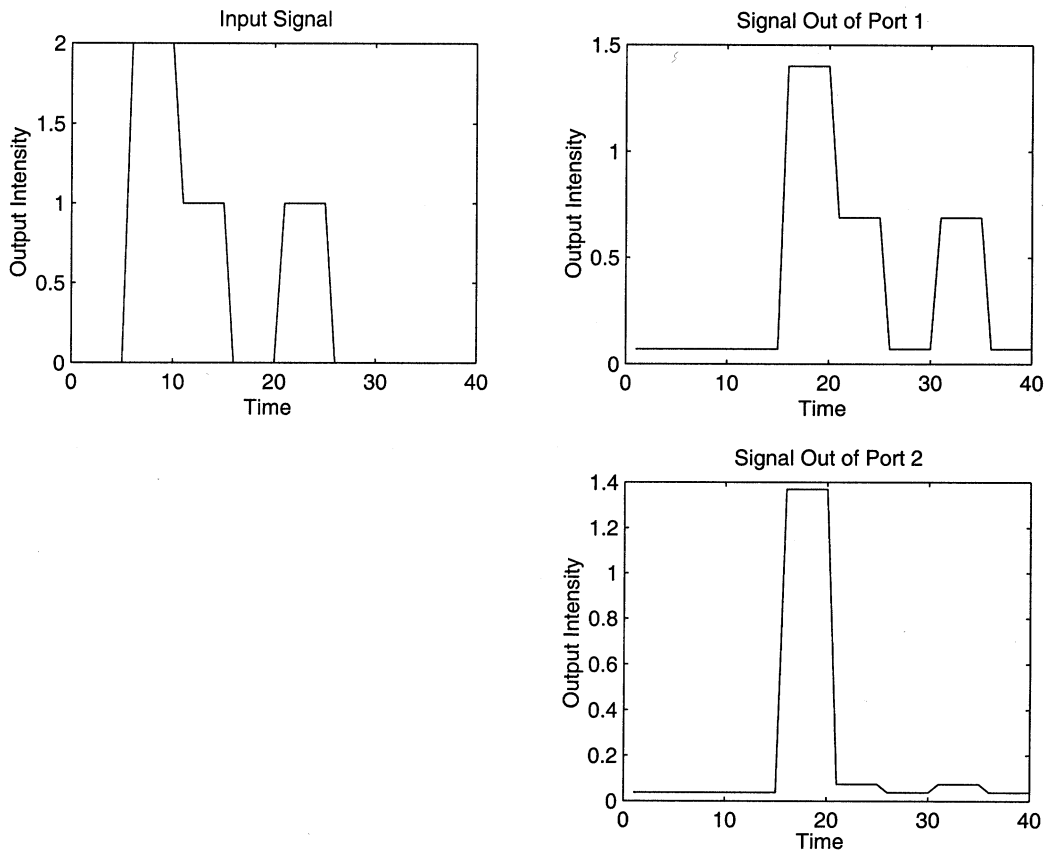
Fig. 13. Input and output signals for a one-bit packet forwarder simulated with parameters corresponding to 800-layer limiter with loss parameters of DPOP-PPV.
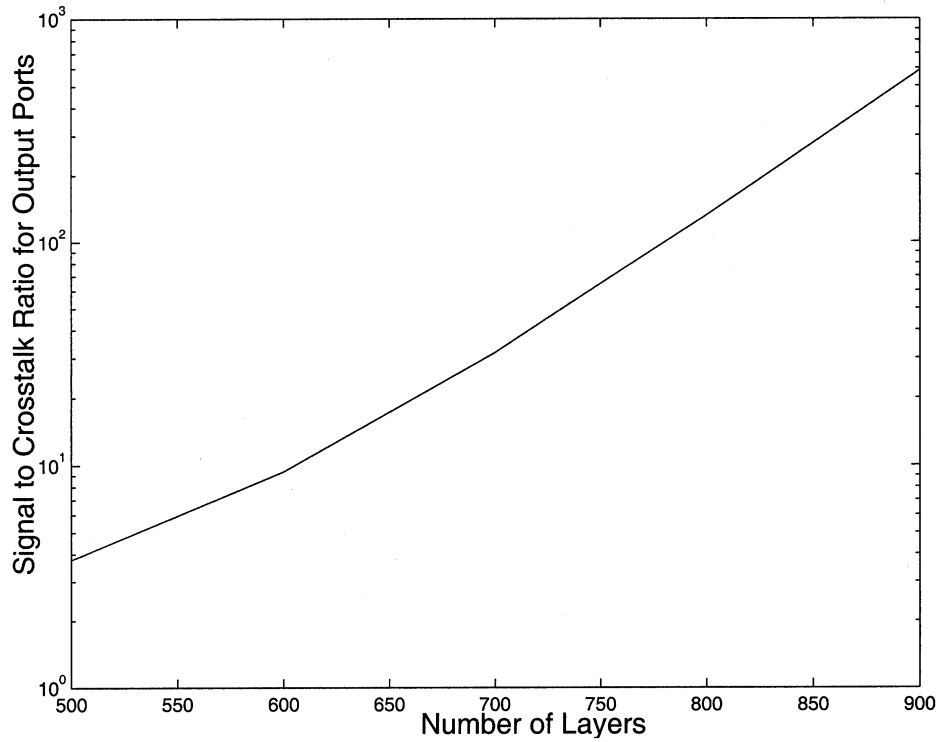

Fig. 14. Signal-to-crosstalk ratio for one-bit packet forwarder for different numbers of layers with loss parameters of DPOP-PPV.

V. Conclusion

We have analyzed noncoherent addition-based signal-processing designs based on a simple basis set of signal transfer functions. The sensitivity of this design scheme to device and signal variations was quantified. We showed that a consequence of using noncoherent addition in sampler design results in an incomplete suppression of input fluctuations. The transfer function smoothness that sufficiently suppressed undesired input signals was seen to correspond to a limiter model with more than 400 layers. As well, the performance of the packet forwarder design was shown to be capped by the capability of the sampler. The best acheivable crosstalk-to-noise ratio was set by the maximum length of lossy device that still provided sampling.

Although the designs were analyzed in the context of an all-optical device, the results are applicable to any device that provides such a set of transfer functions and allows the simple, noncoherent addition of signals.

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Currently, he holds the Nortel Networks Canada Research Chair in Nanotechnology with the University of Toronto. In 2001, in appointing him to the Canada Research Chair, the CRC Foundation wrote, "Sargent has shown that a new kind of photonic macrocrystal,—one which harnesses nature's underlying drive toward symmetry,—will transform how communication networks are built. He has developed the photonic heterostructure."

In 1999, Dr. Sargent was honored with the Silver Medal by the National Sciences and Engineering Research Council of Canada (NSERC), noting, "This work shed light for the very first time on the essential physical mechanisms that underlie the operation of the lateral current laser. The groundbreaking research proved that it is possible to build and interconnect these laser devices using standard semiconductor fabrication techniques, thereby opening up an avenue for making laser light the driving force of future microchips." In 1999, the Ontario Premier's Research Excellence Award committee noted, "Dr. Sargent is innovating revolutionary ways to send, display, and acquire information using light. Dr. Sargent developed the theory and demonstrated the realization of the lateral current injection laser, a new semiconductor laser with the potential to enable the integration of many optoelectronic devices onto a single platform." In 2000, in awarding him the D. N. Chorafas Award, the Switzerland-based foundation wrote, "Dr. Sargent proved that it is possible to harness the combined power of photons and electrons to make new integrated, functionally sophisticated devices and circuits to enable the fiber-optic networks of the future." In 2002, he was honored by the Canadian Institute for Advanced Research as one of Canada's top 20 researchers under age 40.